CIRCUIT TO DETECT CLOCK DELAY AND METHOD THEREOF

Abstract of the Disclosure

Provided are a circuit and a method of detecting clock delay where the circuit to detect clock delay includes a delay detection circuit and a clock forwarding circuit, the delay detection circuit detects a delay between a predetermined output clock signal and an input clock signal, if the detected delays are identical to one another, the circuit generates an initial parameter corresponding to the delay and if the detected delays are not identical to one another, continuously detects the delay until the detected delays are identical to one another, and generates a reset control signal in response to a system reset signal or a predetermined internal reset signal; the clock forwarding circuit loads and unloads the input data in response to the initial parameter, the circuit to detect clock delay can automatically detect the clock delay necessary for setting the initial parameter of the clock forwarding circuit and reset a master circuit and an external circuit that interfaces with the master circuit, thus performing data transmission without any errors.